

Fig. 1

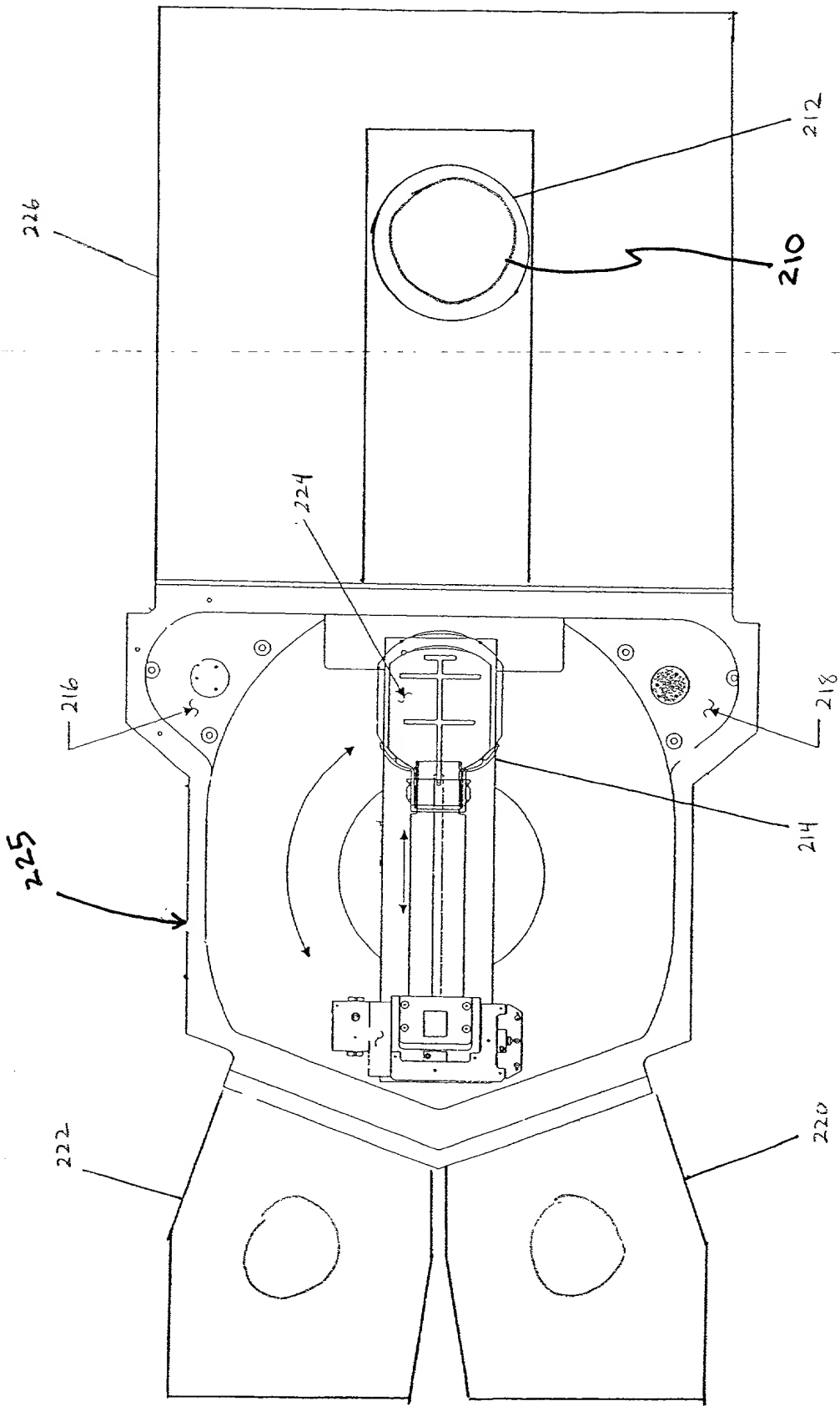


FIG. 2A

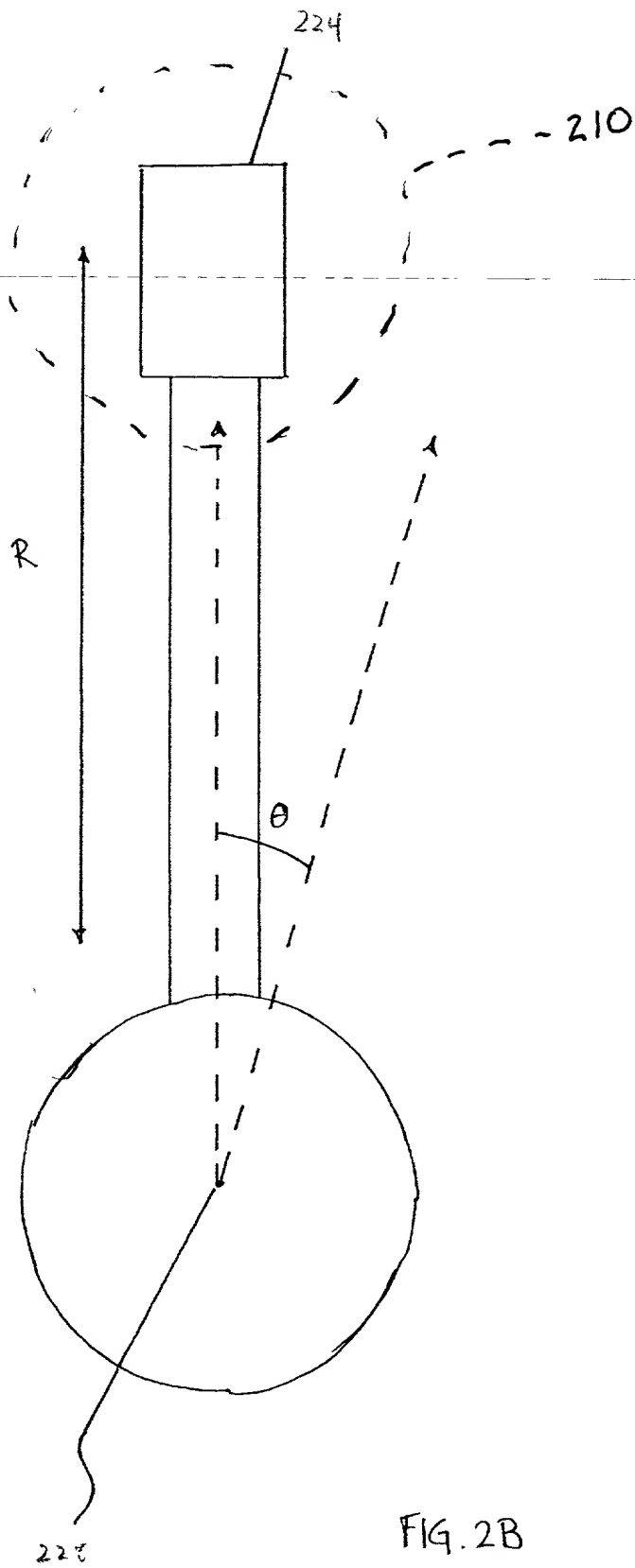


FIG. 2B

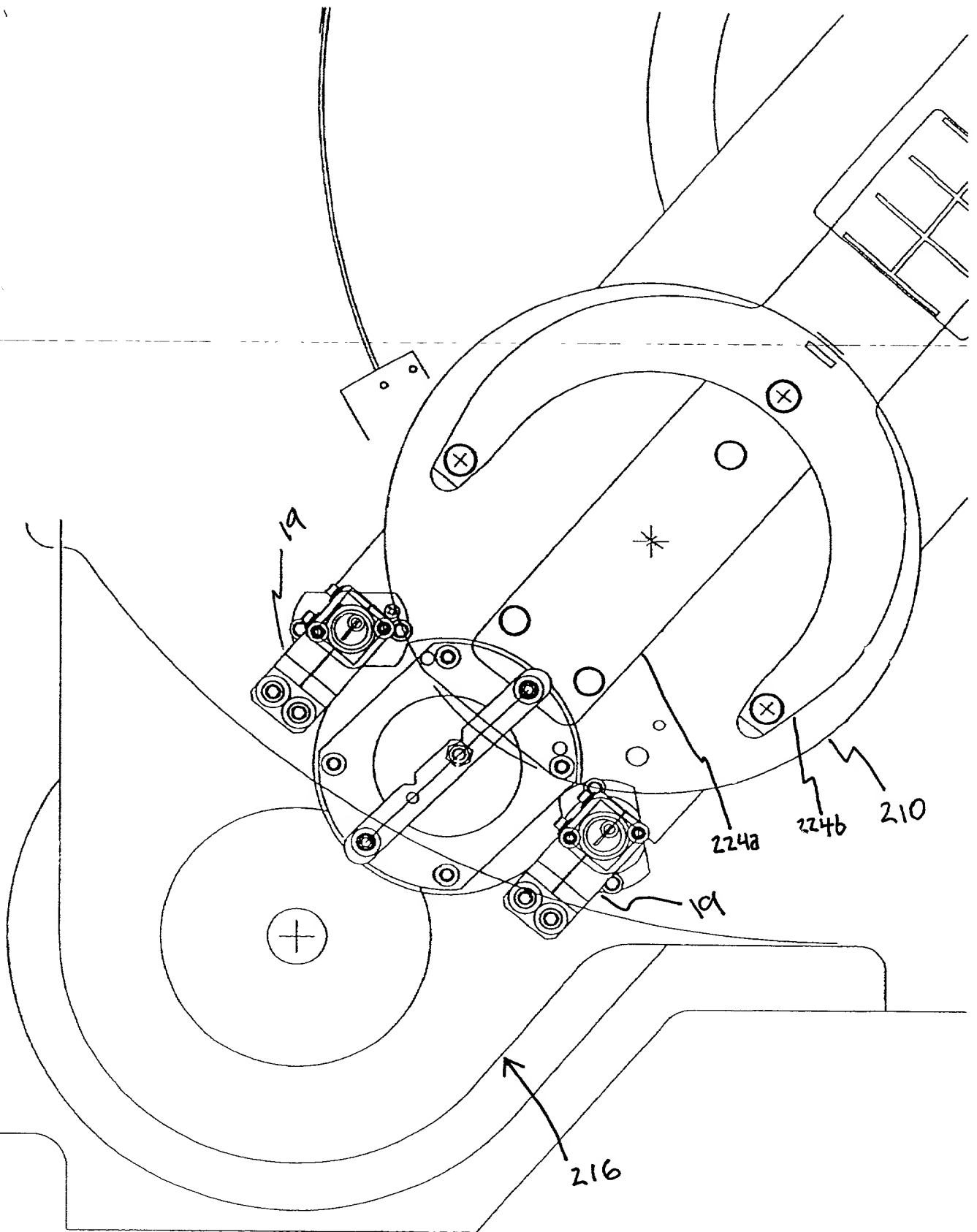


FIG. 2C

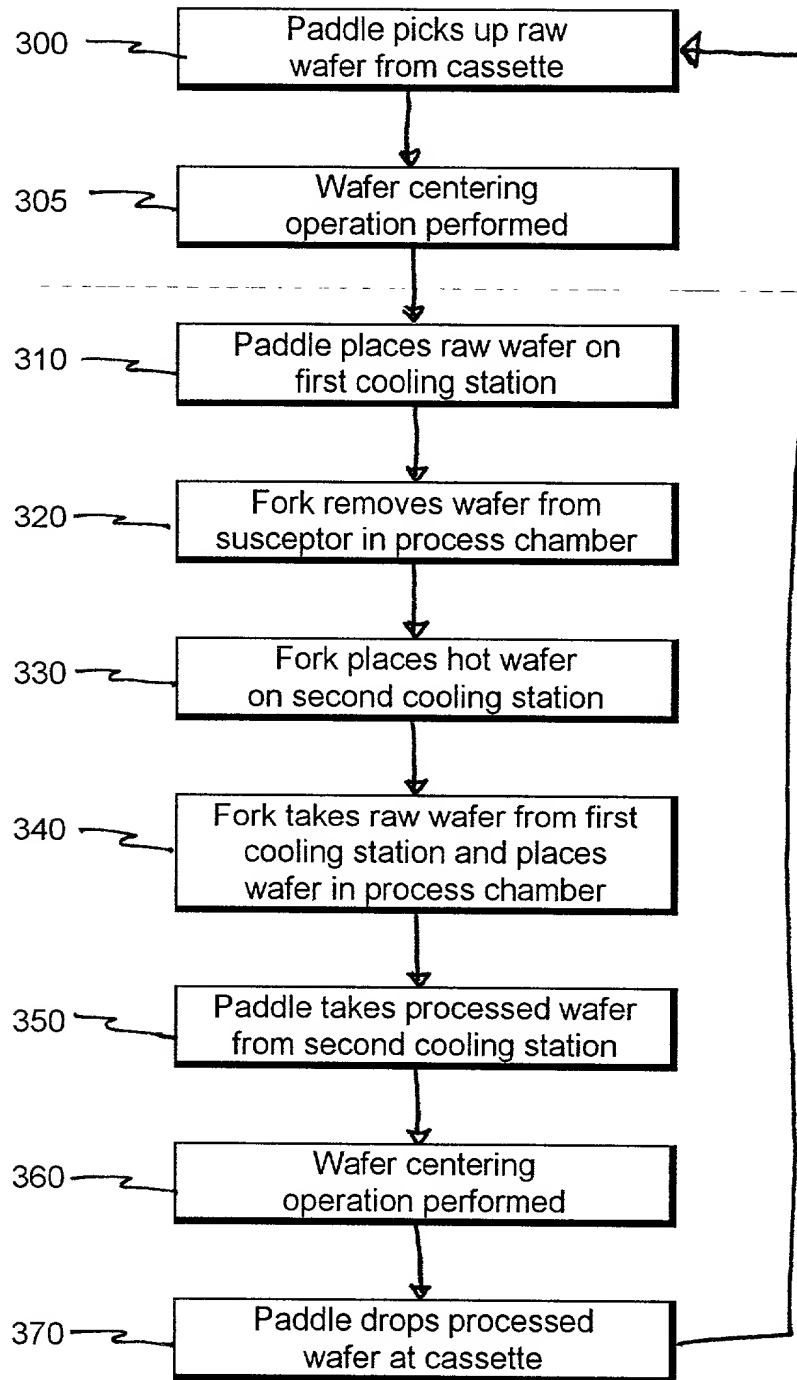


FIG. 3

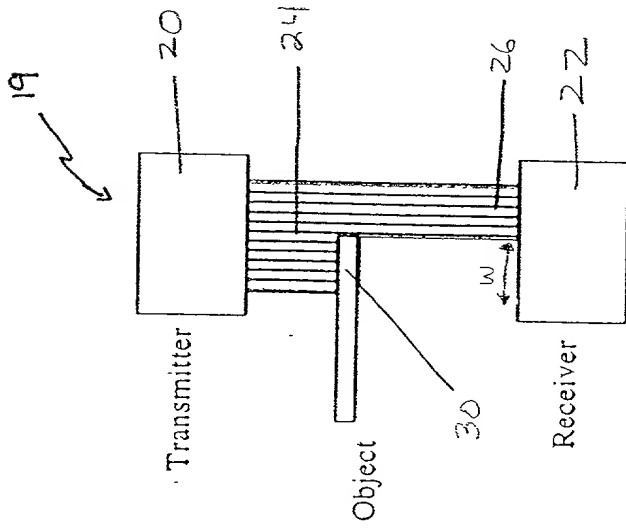


Fig 4
Longitudinal

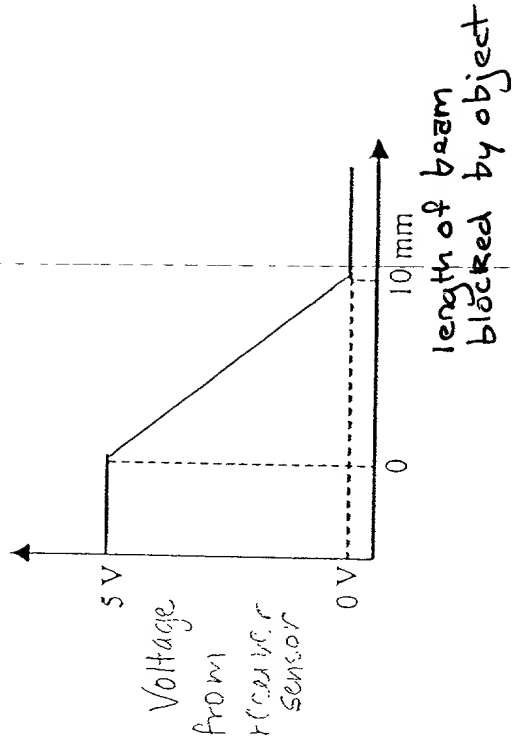


Fig 5

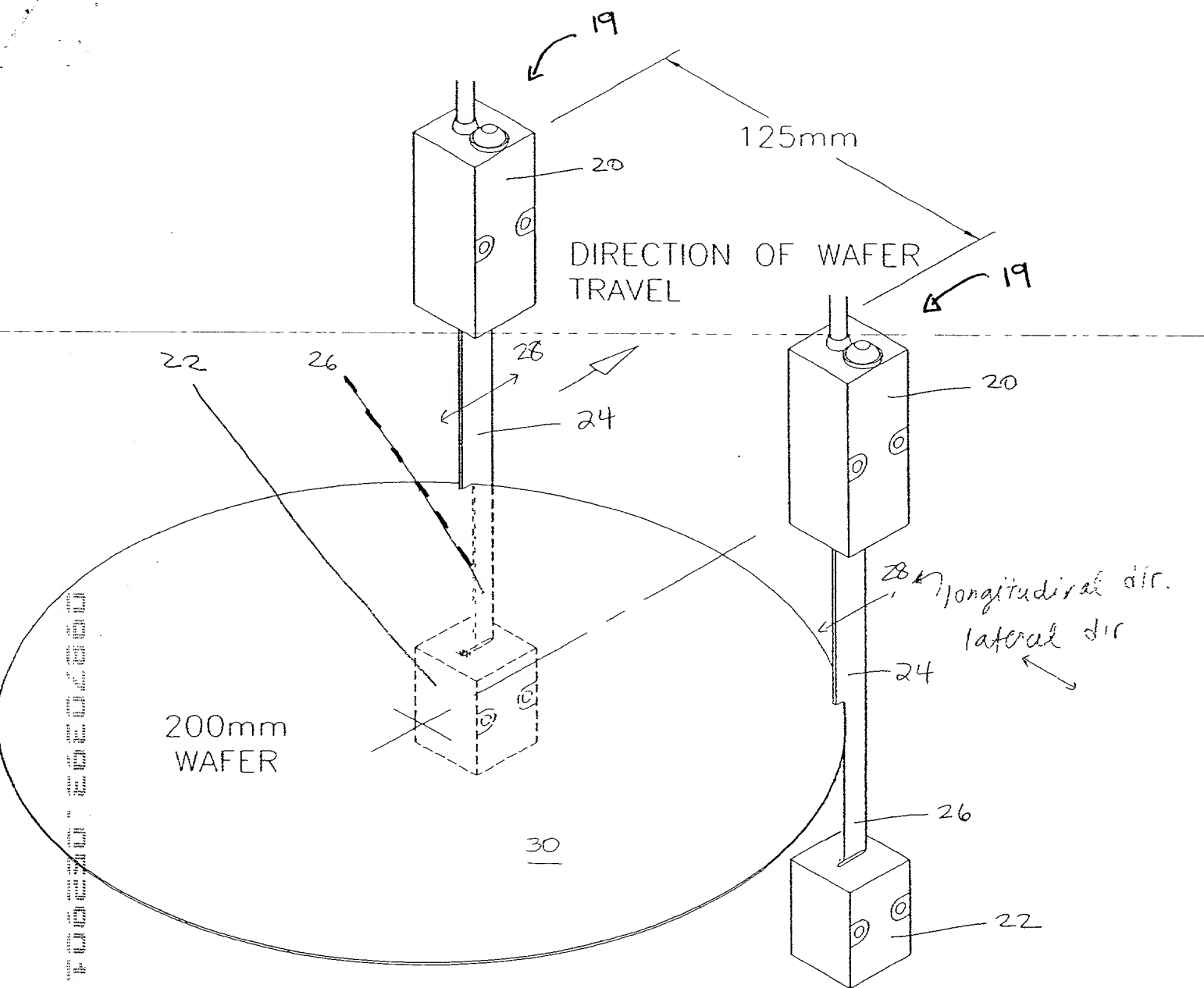


Fig. 6

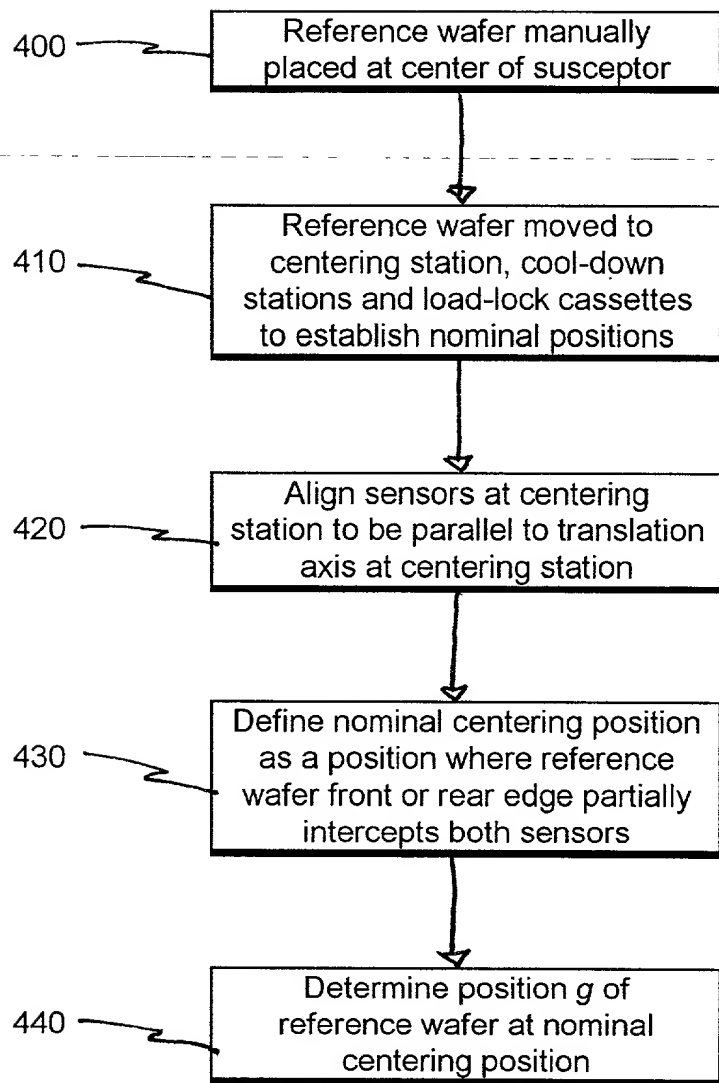


FIG. 7

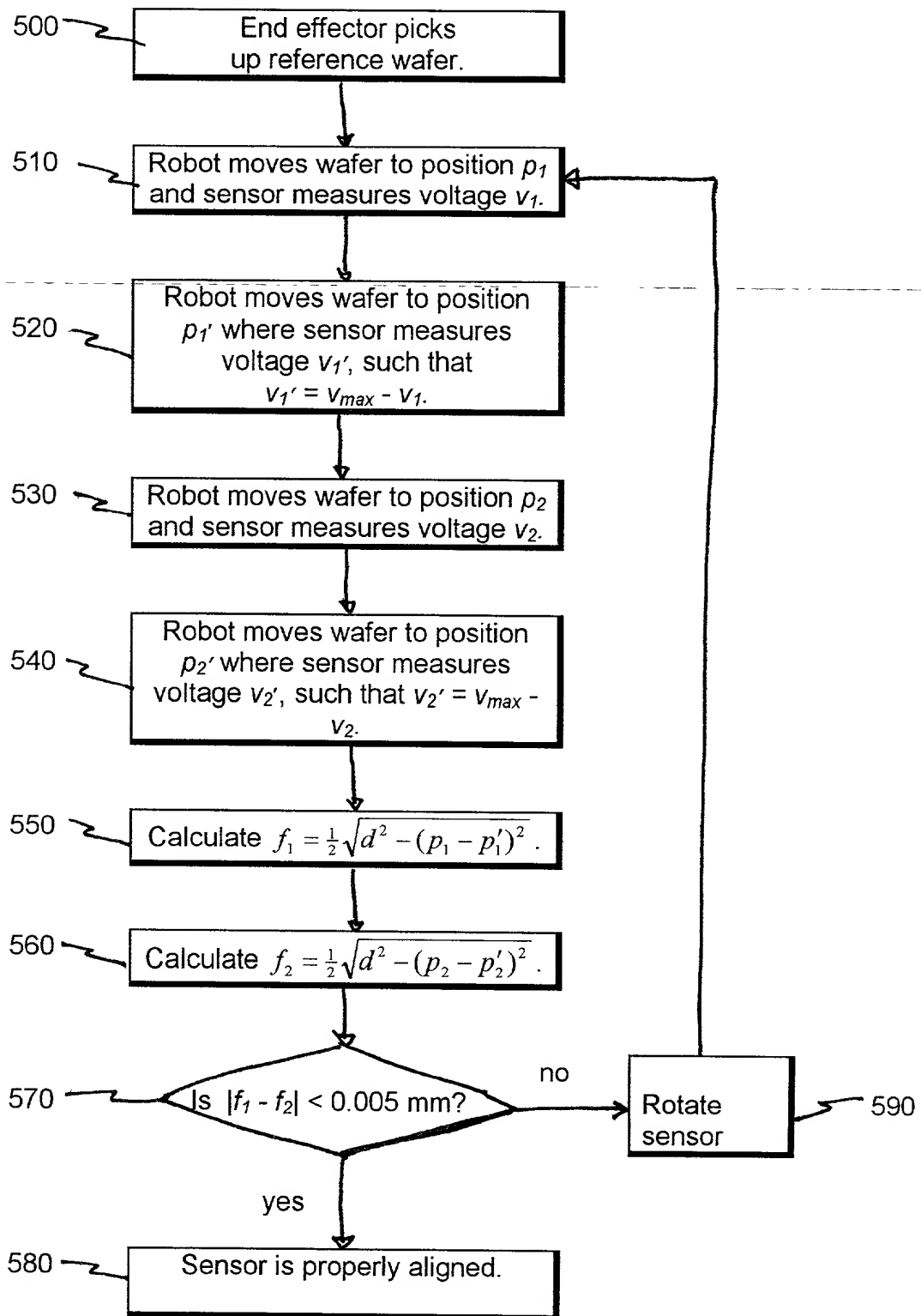


FIG. 8

FIG. 9

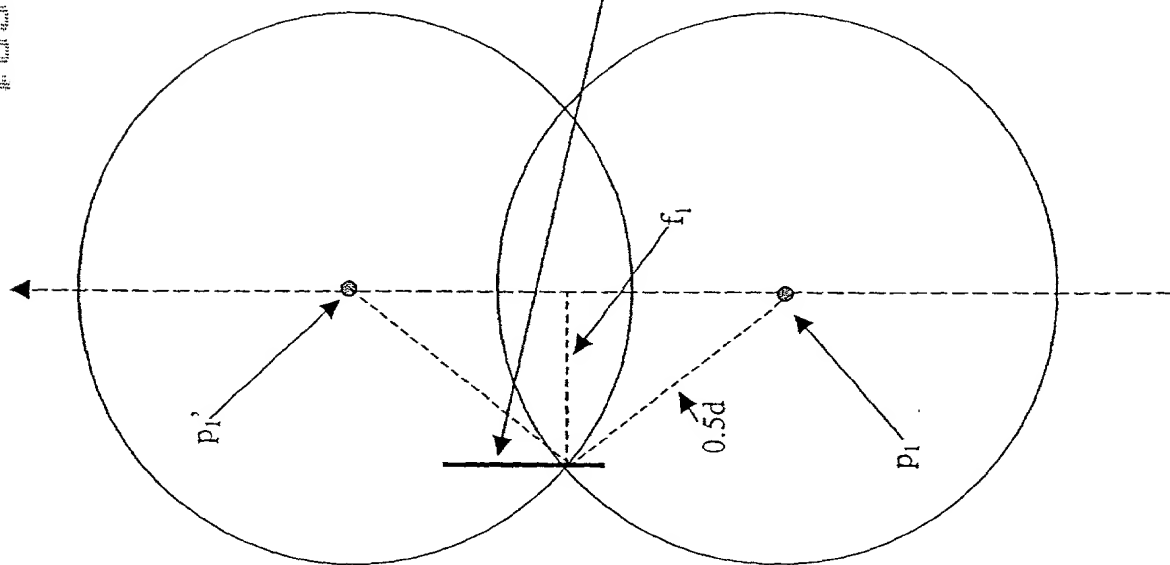


FIG. 9

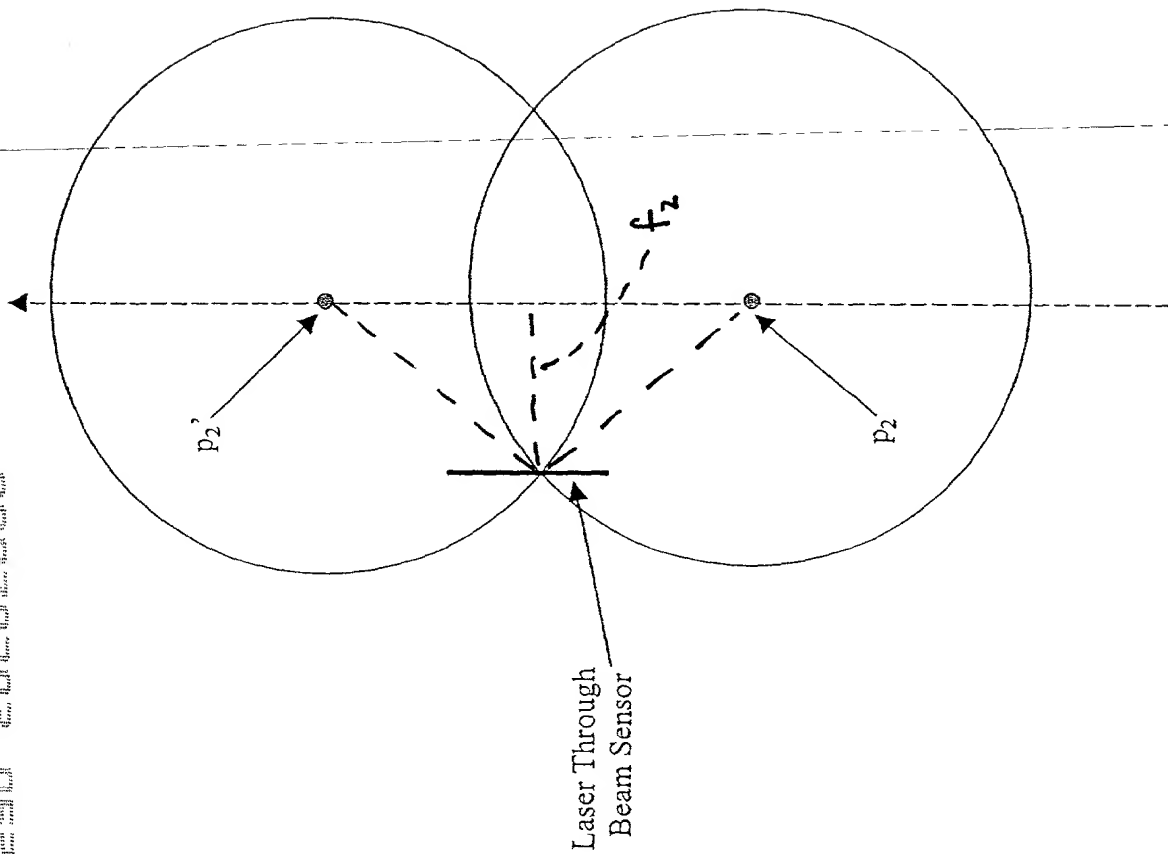


FIG. 10

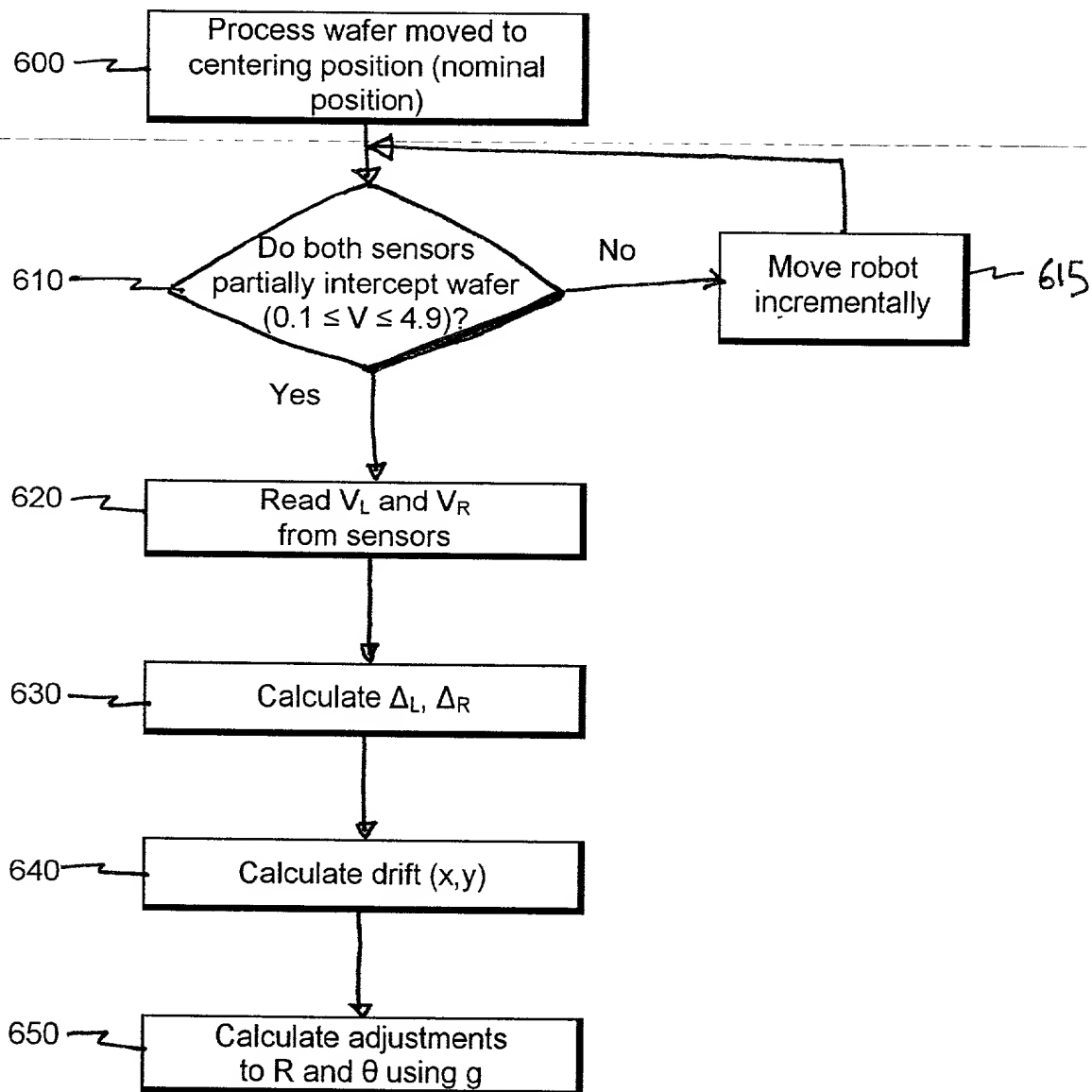


FIG. 11

Wafer Position/Error Calculation

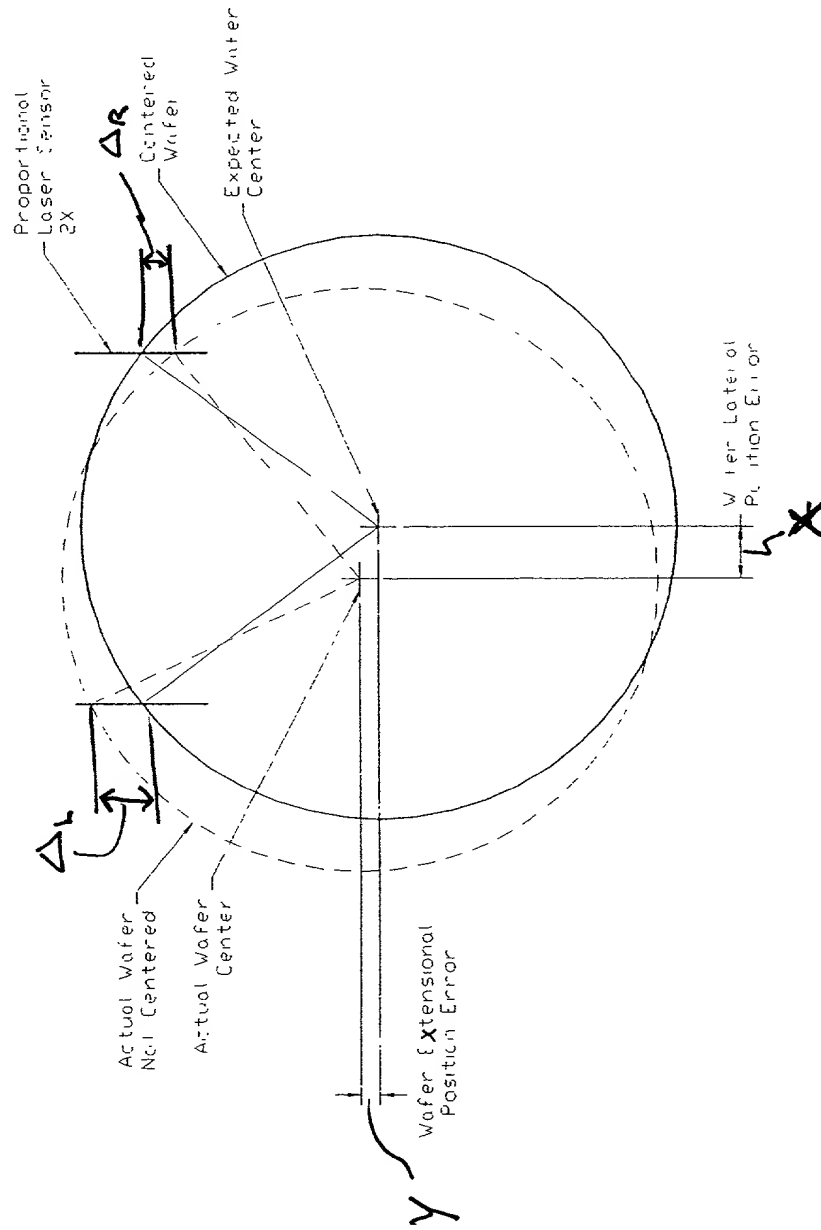


FIG. 12